ReRAM Compute ASIC Fabrication

Team: Sddec24-13
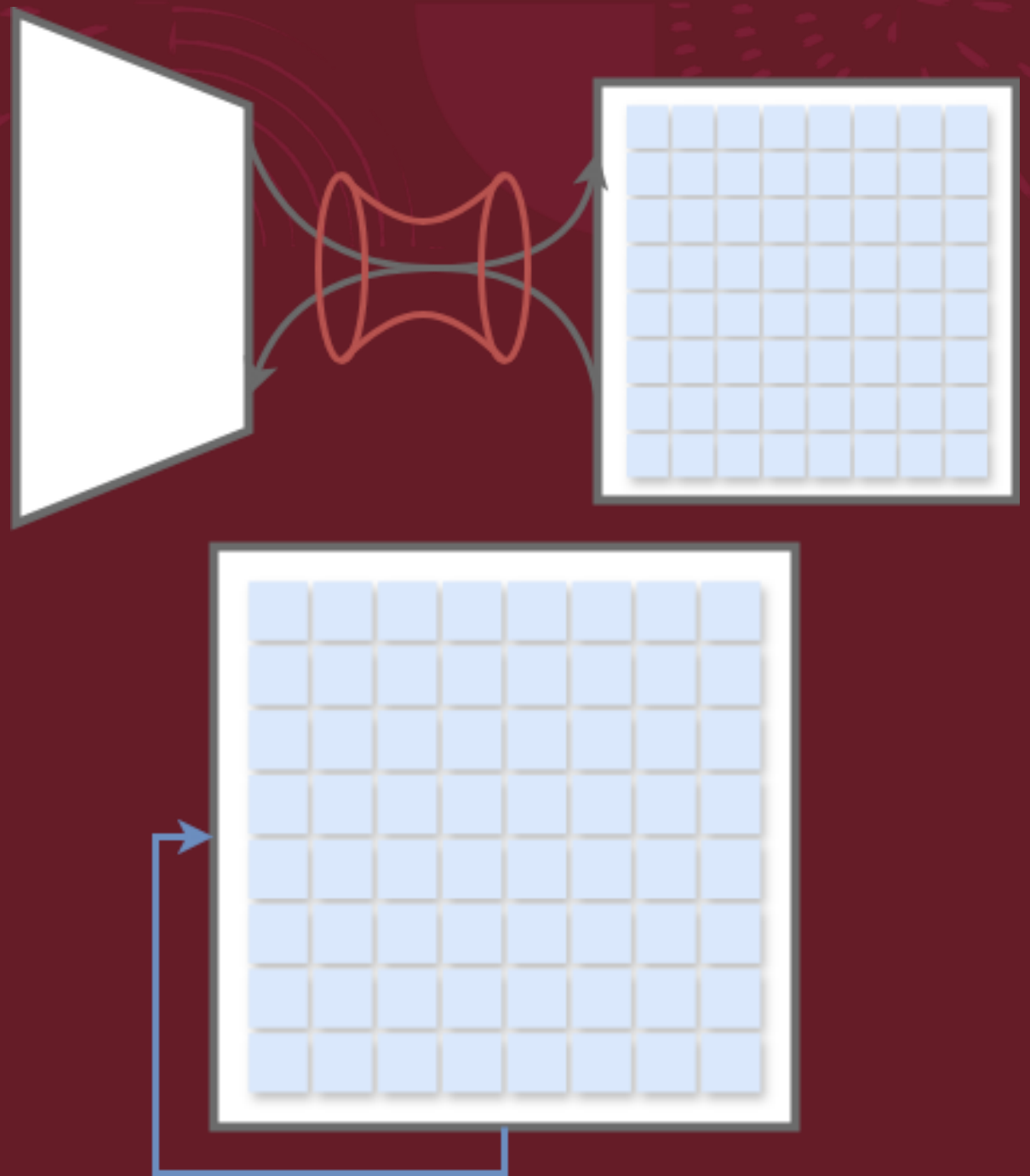
Members: Konnor Kivimagi, Jason Xie, Gage Moorman, Nathan Cook

Client: Dr. Henry Duwe
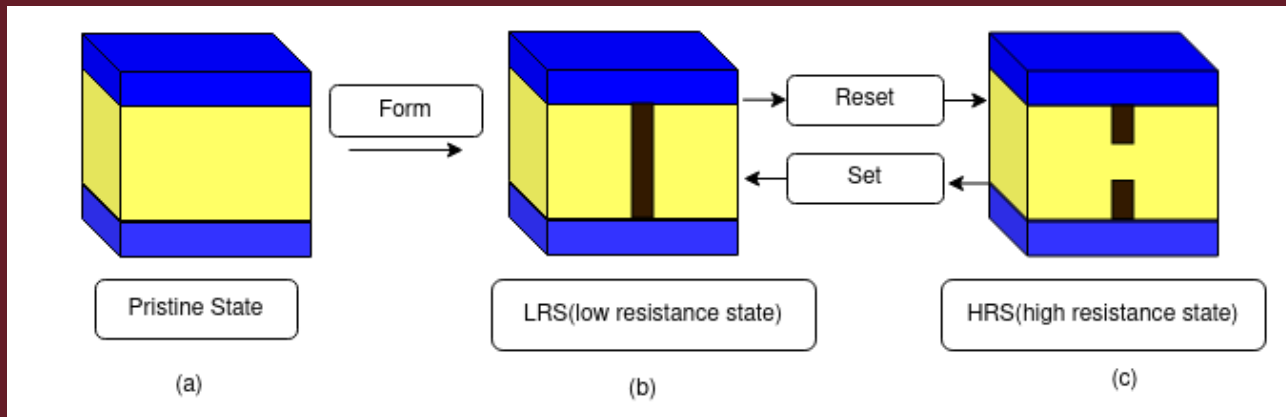
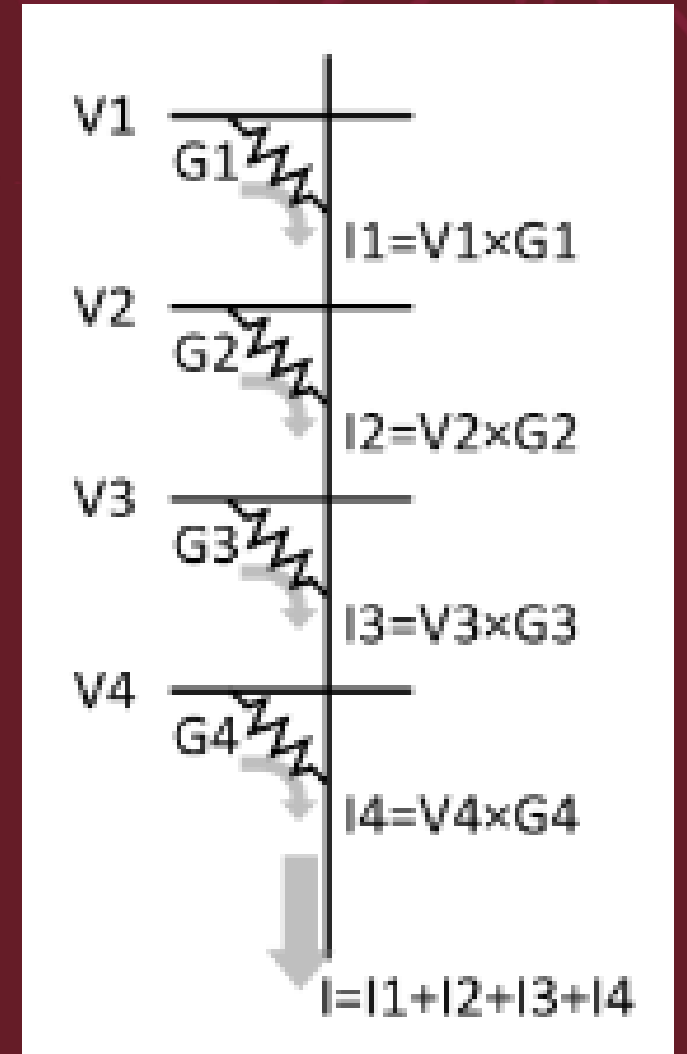Advisor: Dr. Cheng Wang

Broad context

- Machine learning...
  - Bottlenecked by data transfer from memory to CPU
- In memory computation using matrix multiplication can solve the bottleneck

ReRAM

How ReRAM works

Source 2

ReRAM MAC

3

ReRAM pros and cons

Pros	Cons
High memory density	Variation due to random noise
Non-volatile memory	Different manufacturing process
Low power consumption	Not an established technology
Ability to scale to smaller processes	

Problem Statement

- Problem statement
    - Create a research vehicle for silicon proving computational resistive random access memory for research and educational purposes
- Goals
    - Create a design to be fabricated through the Efabless ChipIgnite program
    - Create documentation for future students to be able to test our design
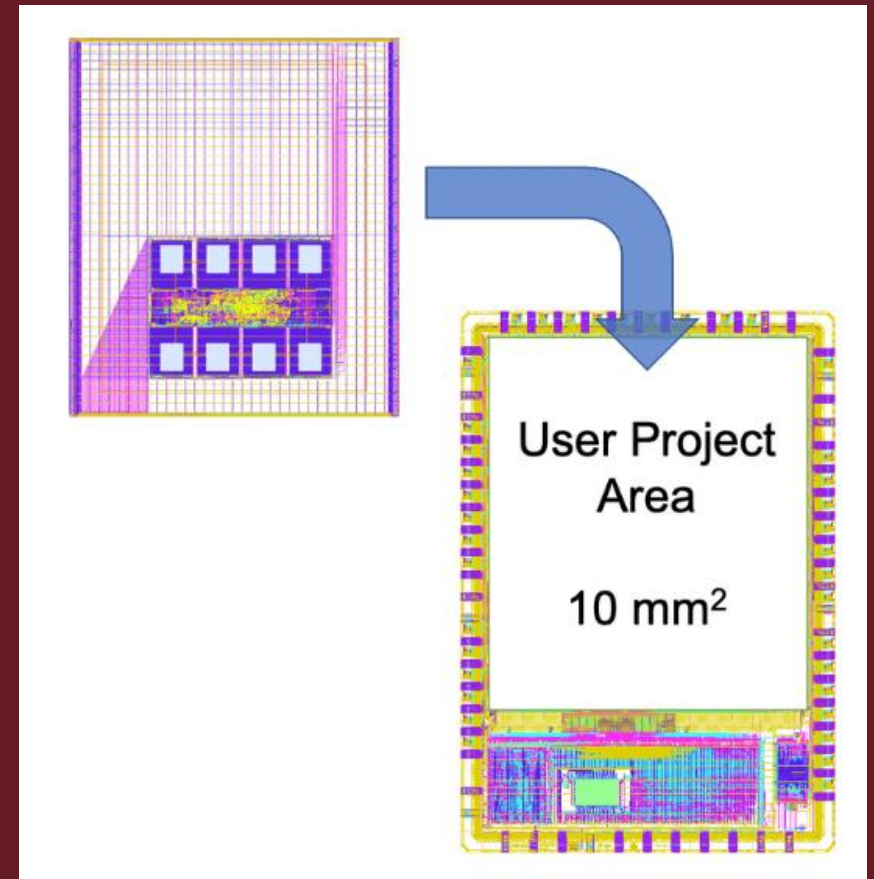
Efabless Fabrication

Efabless runs a shuttle program every few months
- Low cost development
- Projects are required to be open-source
- Uses Skywater 130nm process

Design Process
- Create a design
- Integrate it into the caravel harness
- Submit for fabrication


Source 1

Users

- Graduate Students
  - Documentation on Efabless process and tool flow
- Undergrad Students
  - Easy to follow lab documentation
  - Gain the ability to bring up a chip in parallel with their regular coursework
- Professor Duwe and Professor Wang
  - Practical example of a crossbar for research and testing
  - Provide valuable resources for the co-curricular chip program

Requirements

- Functional Requirements
  - Design an 8x8 ReRAM crossbar that can perform matrix vector multiplication
  - Create an ADC with a sufficient resolution
  - 1MHz clock speed
  - Minimize area

- Non-functional Requirements
  - Project Documentation
  - Bring-up plan for testing the fabricated chip

Top level design

- Control circuits – Logic analyzer, row, power, and column select, decides what operation is performed

- DAC – used during standalone operation

- Power select – selects the voltage values being used

- ADC and TIA network – Convert ReRAM analog output to a logic analyzer compatible digital output
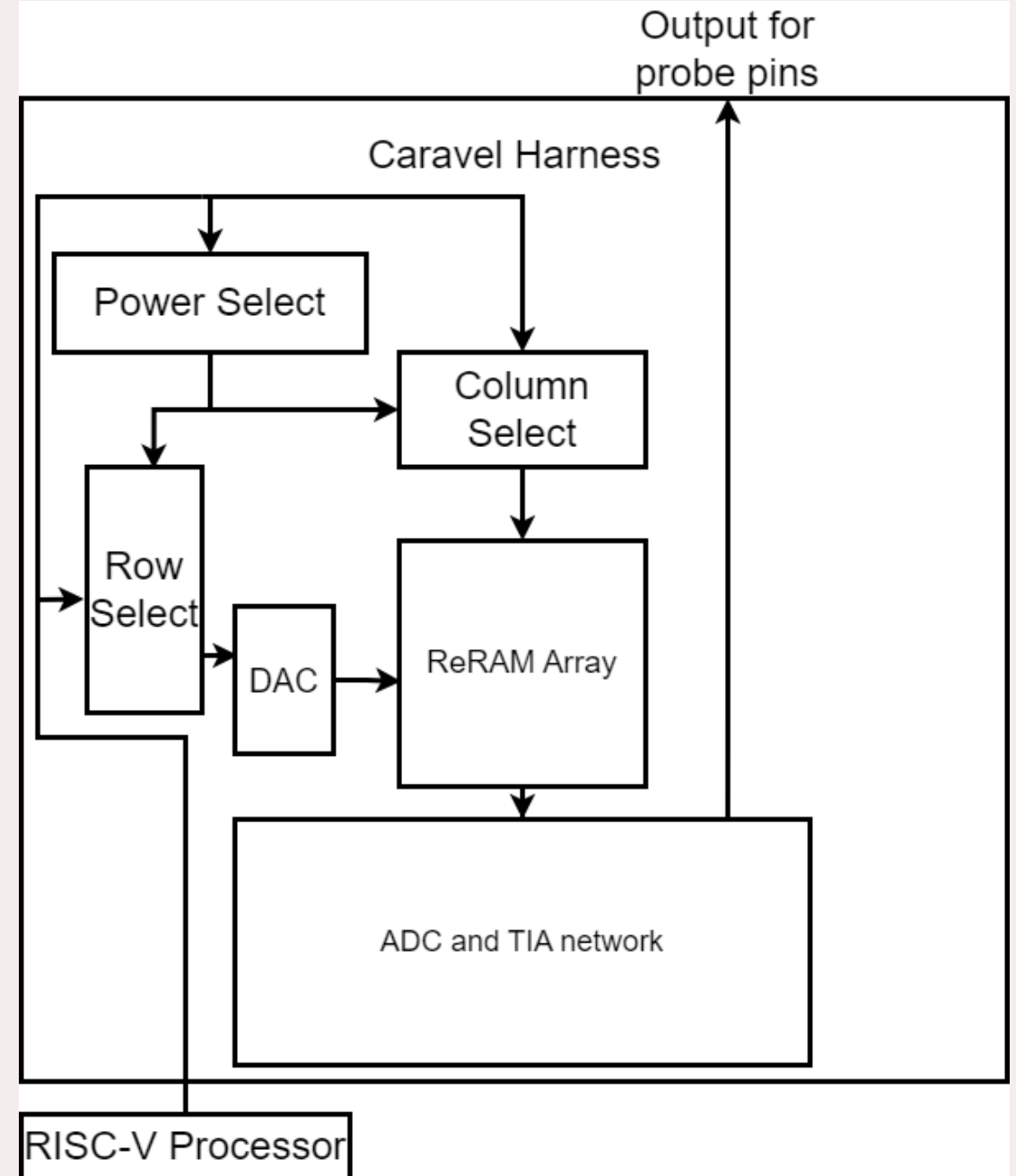
ReRAM operations

Write

- Bitline selects column
  - Also chooses the written value
- Wordline selects row
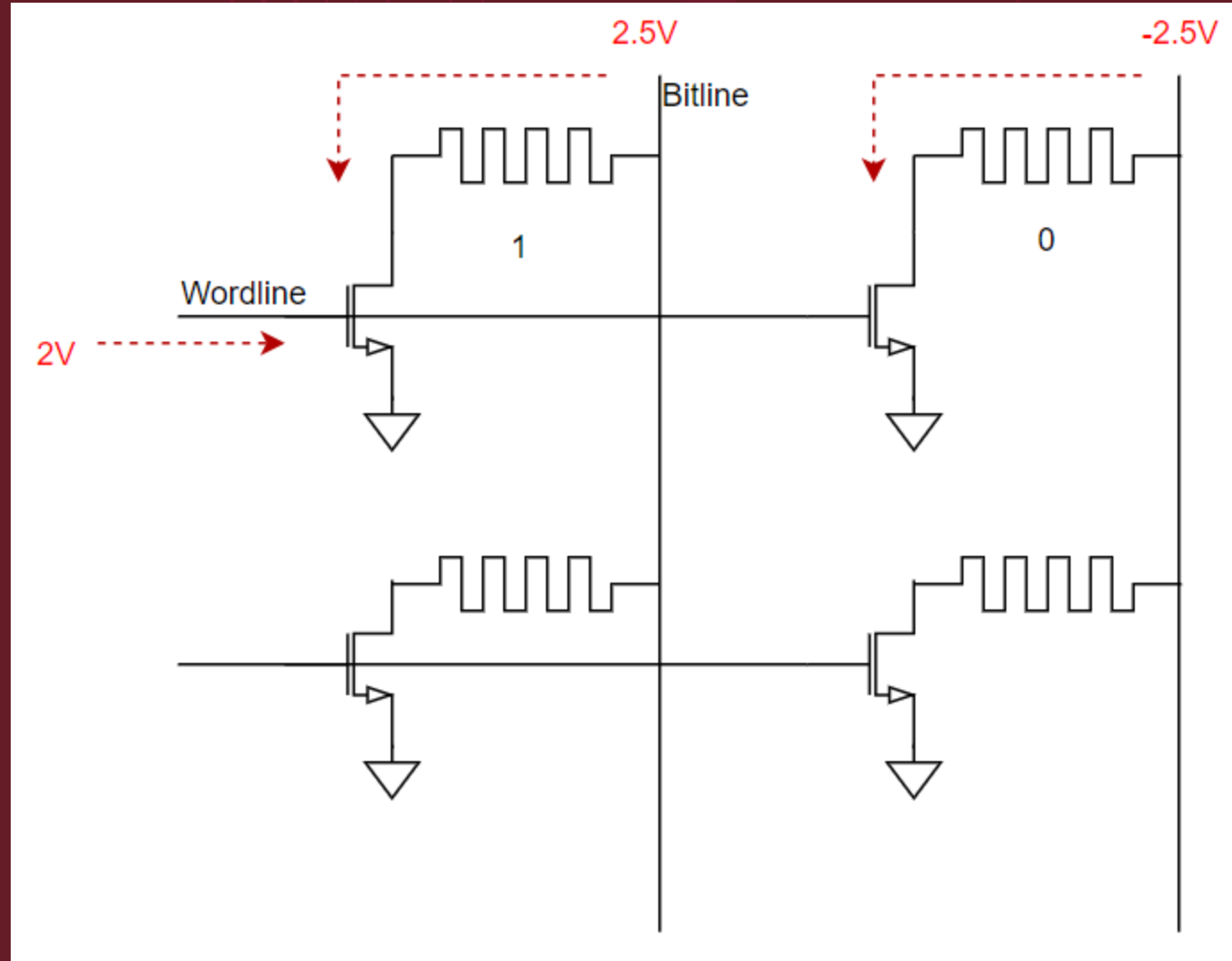
ReRAM Operations

MAC/read

- Currents add
- Resistor multiplies
  - $I = VG$
  - $G = 1/R$
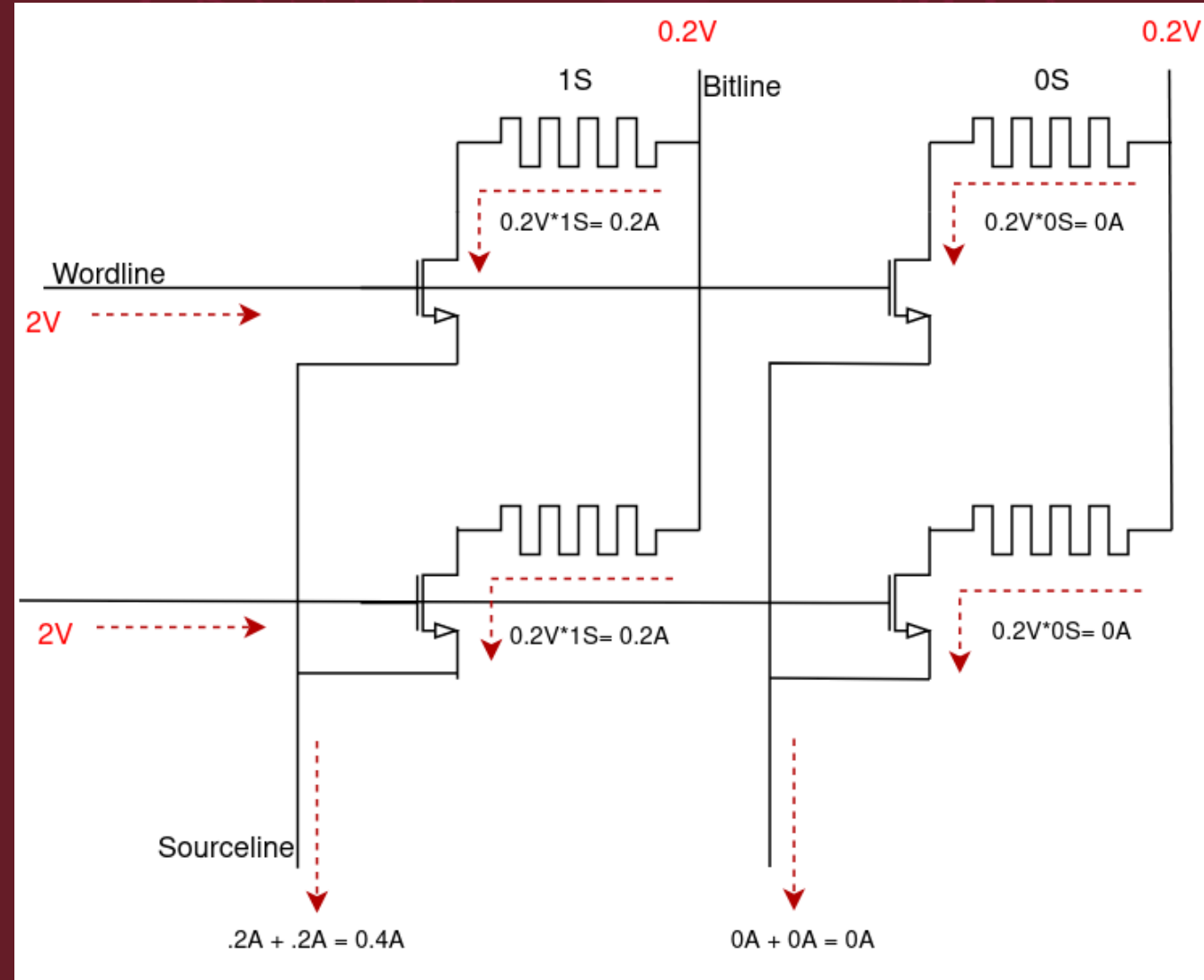
ADC

- Flash ADC
  - Simple
  - Fast
- 4-bit resoultion
- SNR 25.84 dB
- Other testing still in progress
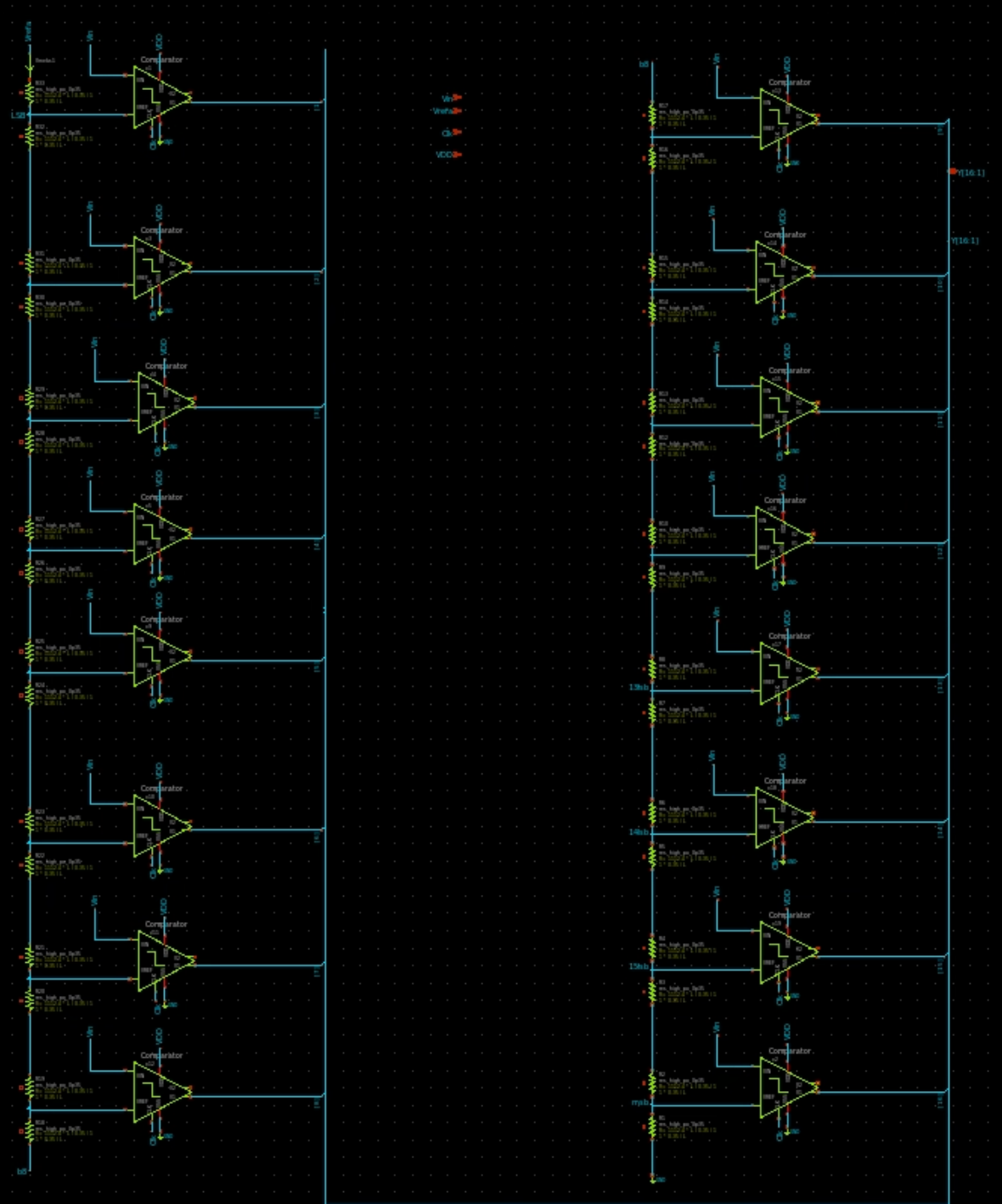
Comparator

- StrongARM Comparator
  - Zero static power consumption
  - Rail to rail outputs
  - Reduction in input referred offset voltage
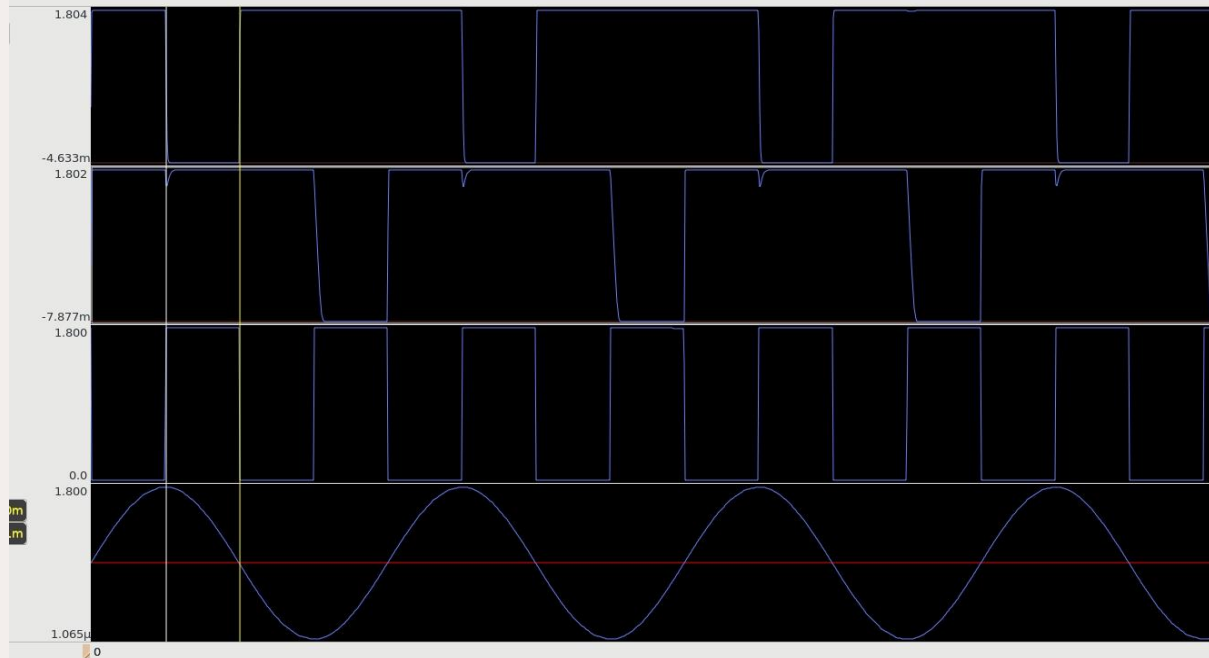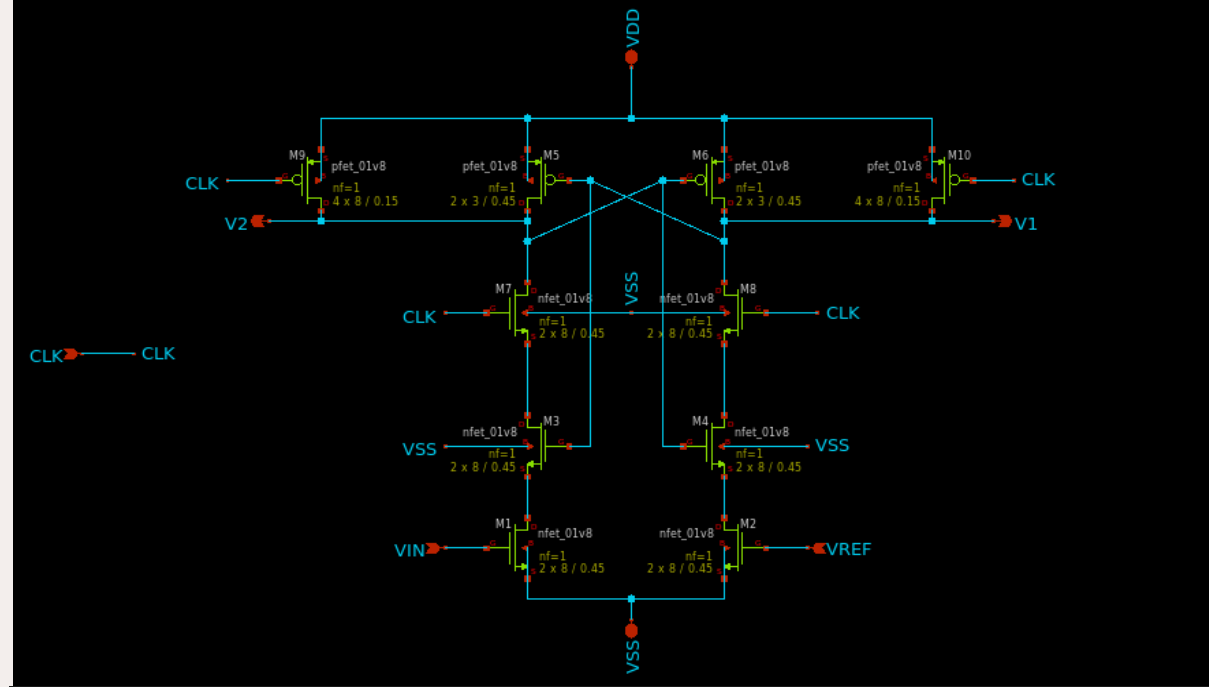
Priority Encoder

- Used for thermometer to binary encoding

- One-hot encoding

- Fully digital component
  - To be implemented with OpenLane "blackboxing"
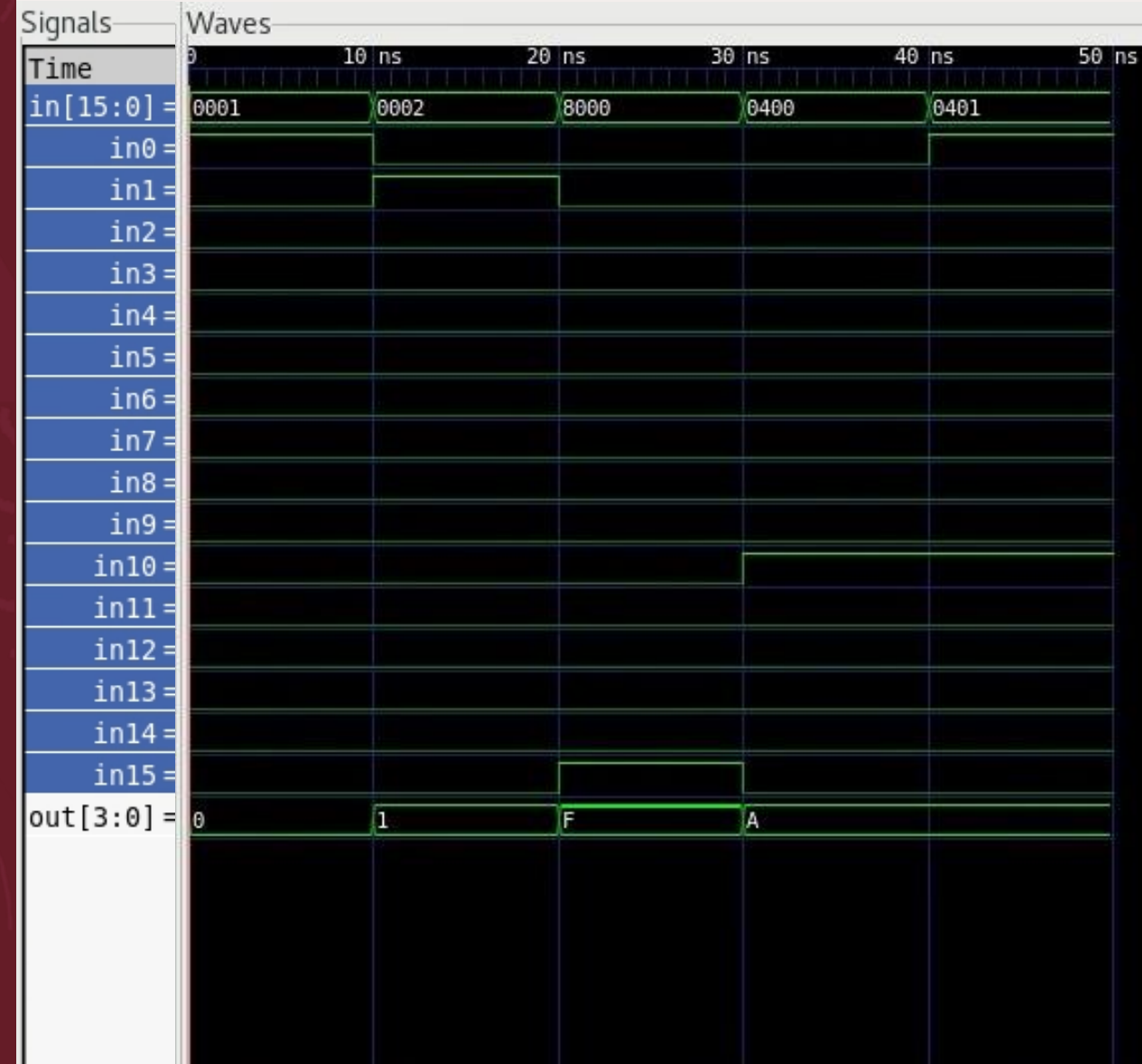
TIA

- 5T op-amp with feedback resistor
  - Very simple to implement
  - Insufficient input swing
- 7T op-amp with feedback resistor
  - Requires a capacitor
  - Reasonable input swing
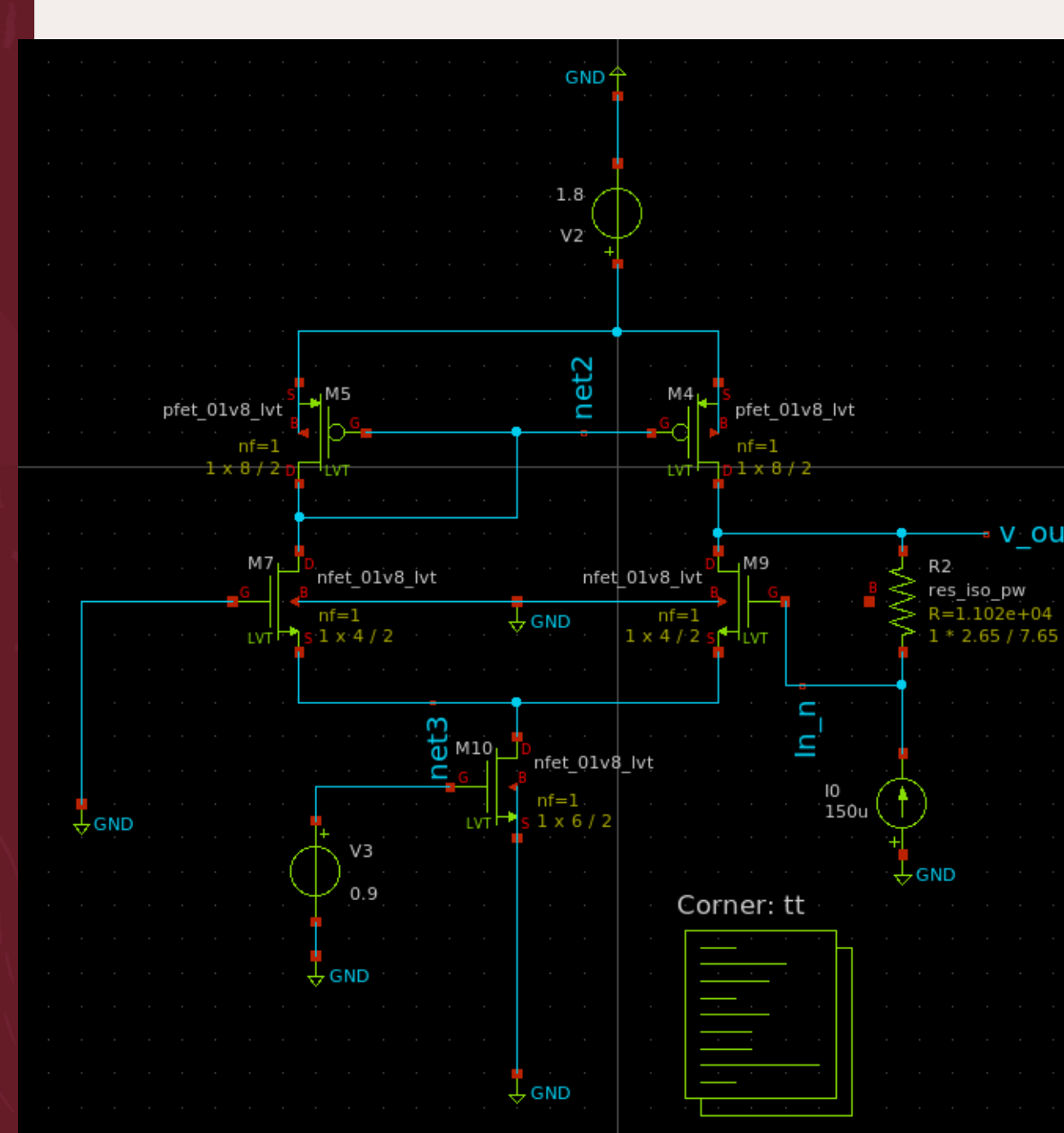
Risk Mitigation

- Peripheral Circuits Delay
  - Risk: Peripheral circuits may not be completed on time.
  - Mitigation: Thorough planning, use of Cadence, simplification of designs.
- Memristor and CMOS Modeling Issues
  - Risk: Inaccurate memristor model and inconsistent CMOS transistor simulation.
  - Mitigation: Explore open-source SPICE models, document current issues, propose future solutions.
- Fabrication Errors
  - Risk: Design constraints not met due to fabrication errors.
  - Mitigation: Detailed bring-up plan with testing methods, acknowledge limitations in preventing fabrication errors.

Design Tools

- Xschem - Schematic capture

- Netgen – Used for LVS

- Ngspice – Spice simulator

- Magic - Layout creation

- Klayout – GDSII viewer

- GTKwave – Verilog waveforms

Testing Plan

Schematic in Xschem

Unit test in Verilog

Develop and test components

Conduct mismatch corners

Synthesize in OpenLane

Generate netlist in Magic VLSI

Prepare for mixed-signal testing

Test systemic functionality

Top-level component design and test

Develop layout in Magic VLSI

Pass DRC and LVS checks

Finalize layout

Run PEX

Analog simulation with parasitic capacitance

Parasitic capacitance extraction

Integrate user project into Caravel Harness

Pass MPW-precheck

Caravel Harness integration

Project Status

Component	Planning	Design	Testing	Layout
DAC	🟩	🟩	🟩	🟩
ADC	🟩	🟨		
TIA	🟩	🟩	🟨	
ReRAM Crossbar	🟩	🟩	🟨	
Control circuits	🟨			

Immediate next steps:

- Finalize ADC components

- Conduct ADC and TIA testing

- Complete full ReRAM array

- Contribute to co-curricular ChipFab documentation

- Verify control instruction sets

Timeline

Tasks	STATUS	Jan	Feb	Mar	Apr	May	June	July	Aug	Sep	Oct	Nov	Dec
Phase 1: Tool setup / ReRAM research	STATUS												
Learn about open source tools	Done												
Learn how ReRAM works and its benefits	Done												
Phase 2: Project and component research													
Research architectures for ADC and TIA	Done												
Determine the best way to interface with our design	Done												
Research ReRAM crossbar architectures	Done												
Phase 3: Component design and verification													
Create schematics	In Progress												
Create layouts													
Each circuit must pass both DRC and LVS													
Phase 4: Integration of all components													
Create a top-level schematic													
Create a top-level layout													
Top-level design passes LVS													
Testing to verify design fuctionality and find mistakes													
Circuit passes MPW precheck													
Phase 5: Finalize													
Create design documentation	In Progress												
Create a bring-up plan													
Submit our design to Efabless MPW													

Work Breakdown

Gage Moorman

- ADC design

Konnor Kivimagi

- Analog tool setup

- ReRAM design

Jason Xie

- Digital tool setup

- TIA design

Nathan Cook

- Control circuits design

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Conclusion

Accomplishments:

- Analog design toolflow
- Digital design toolflow

Component progress:

- DAC realization
- ADC architecture research
- ReRAM crossbar operation and simulation
- TIA parameter extraction

Plans for next semester:

- Mixed signal integration
- Finish sizing ADC and TIA
- Complete control circuitry
- Develop bringup test plan
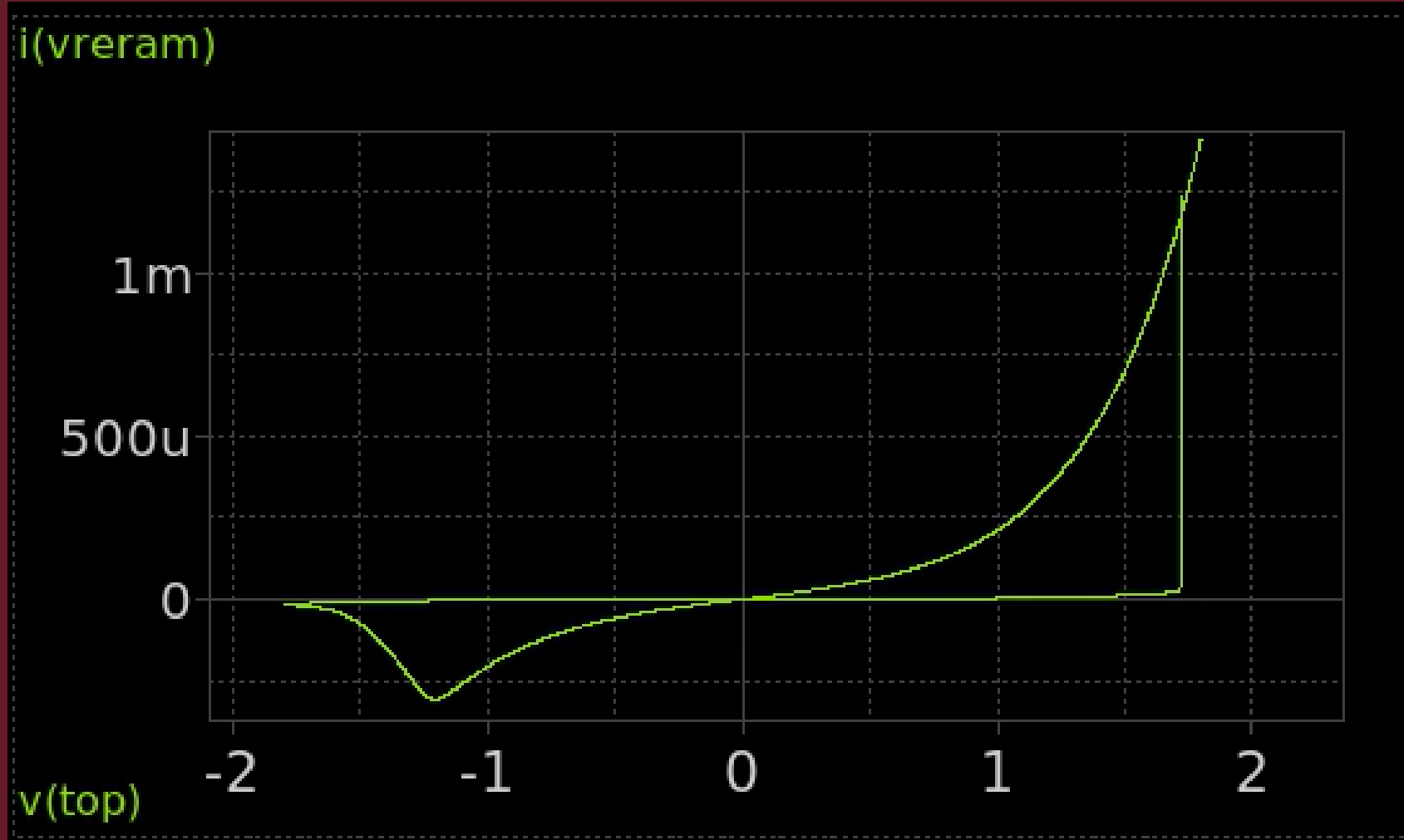- Update documentation

Questions?

Supplementary Slides

Definitions

- DRC : Design Rule Check

- LVS: Layout vs Schematic

- MPW: Multi-Project Wafer

- Efabless: Chip design company

- ReRAM: Resistive Random Access Memory

- ASIC: Application Specific Integrated Circuit

- ADC: Analogue to Digital Converter

- DAC: Digital to Analogue Converter

- TIA: Transimpedance Amplifier

ReRAM IV Curve

Sources

1) https://efabless.com/chipignite

2) https://web.eecs.umich.edu/~zhengya/papers/chou_micro19.pdf

3) http://opencircuitdesign.com/magic/

4) https://semiwiki.com/semiconductor-manufacturers/tsmc/287672-in-memory-computing-for-low-power-neural-network-inference/

5) Tony Chan Carusone, D. Johns, and K. W. Martin, *Analog integrated circuit design*. Hoboken, Nj Wiley, 2012.

6) B. Razavi, "The StrongARM Latch [A Circuit for All Seasons]," in IEEE Solid-State Circuits Magazine, vol. 7, no. 2, pp. 12-17, Spring 2015, doi: 10.1109/MSSC.2015.2418155.